Multichannel Data Acquisition System for Mapping the Electrical Activity of the Heart

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CIACCIO, E.J., ET AL.: Multichannel Data Acquisition System for Mapping the Electrical Activity of the Heart. ***Background:*** *Details of the electrical conduction pattern of the heart are revealed to the electrophysiologist when multichannel data are used for activation mapping. Commercial electronic systems are available for simultaneous acquisition of many surface electrograms; however, the cost of these systems may be prohibitive and they can be mostly inflexible for adaptation to other research projects. Furthermore, the hardware and software design is often proprietary. In this article we describe the in-house design and implementation of a 320-multichannel acquisition system for animal electrophysiologic research.*

Method and Results: *Several modules comprise this system. The multichannel data are first preprocessed by amplification, filtering, and analog multiplexing. An algorithm for automatic adjustment of signal gains is implemented to maximize the voltage resolution and minimize noise pickup. Signals are then digitized, and sequenced to order the multichannel data and to add markers required for analysis. The digital data are streamed to archival storage media. Additionally, the electrocardiogram (ECG), blood pressure, and stimulus channel signals are stored simultaneously. Selected signals are then displayed in real-time for measurement and analysis and as a check of the system integrity. Examples of multielectrode arrays and surface recordings are provided. Costs for building such a system are estimated.*

Conclusions: *Multichannel data acquisition systems that are designed and constructed in-house have several advantages over turnkey commercial systems, including the potential for considerable cost savings, flexibility in acquiring data, and the ability to subsequently add additional components. (PACE 2005; 28:826–838)*

acquisition, data, electrocardiology, mapping, multichannel, signals

Background

Multichannel data acquisition and cardiac mapping systems are important tools of the electrophysiologist.[1–3] Simultaneous acquisition of many data points recorded at the heart surface and/or from the mid-myocardium are useful to rapidly ascertain the pattern of electrical activation during each cardiac cycle in normal sinus rhythm, pacing, and arrhythmia.[3] For example, in postinfarction hearts, a border zone is formed, which is defined as a thin layer of surviving myocardial cells located in proximity to and often superficial to the infarct location.[4] In human postinfarction patients, the border zone is typically located at the endocardial surface but it can also be transmural.[4] In canine postinfarction experiments the infarct border zone is typically at the epicardial surface.[4] When the border zone is constrained to superficial layers of the heart, strategically placed surface electrodes can capture the salient activity for detection and measurement of abnormally conducting regions.

Once multichannel data are acquired from the heart surface (endocardial or epicardial), it is often projected onto a two-dimensional computerized grid for display.[1,5] This transformation causes some distortion of the original relationship between electrode locations, but it is utilized for convenience and simplicity. When deeper layers of the heart are involved in activation patterns of interest to the electrophysiologist, plunge electrodes may be used so that signals are acquired in three dimensions.[4,6] For experimental research using animal postinfarction models, it is possible to construct a multichannel data acquisition system in-house.[7] In this article we describe the in-house design and implementation of a 320-multichannel acquisition system for animal electrophysiologic research. This system will be of interest to the clinician doing EP studies who would like to understand the basic principles involved in multichannel data acquisition, and who might be considering the construction of such a system for animal research.

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Method

The system design includes the front-end transduction devices, preprocessing and multiplexing of acquired analog signals, analog-to-digital conversion of these signals, time and channel synchronization of the digital data, real-time display of captured signals, and integration of the components to form a turnkey multichannel data acquisition system.

Transduction Devices

From sites on the heart, 312 electrograms are acquired, and auxiliary signals including three-lead electrocardiogram (ECG), blood pressure, and stimulus channel are also recorded (320 channels in total). Electrodes for acquiring heart surface recordings are silver disks. Figure 1 shows an example of a multichannel electrode array under construction. The disk electrodes (~1 mm diameter)[1] are contiguous with the silver leads that are used for connection to the system electronics (panel A). The electrode numbers at the margins from 1–312 are shown. These electrodes are constructed from insulated silver wire, 30–32 AWG. The insulation is removed from the tip of the wire and it is heated in a Bunsen burner to the melting point of silver. A molten ball of metal forms at the tip, which is then manually flattened to form a disk shape. The disk orientation is adjusted so that it is perpendicular to the wire. The electrodes are embedded in a rubbery, durable matrix material (polyurethane) and glued into place on the wire side of the matrix (panel B). Twisted pairs are formed from every two adjacent leads, and each pair will be utilized as a bipolar electrode. A square grid 3 mm on a side was used to embed the electrodes of this array (panel C). Since the electrode disks are ~1 mm, the distance between the pole edges in each bipolar pair is ~2 mm. The distance between the centers of bipolar electrodes will be 3 mm in the horizontal and vertical directions. The shape of the entire recording surface is irregular to conform to the curved epicardial surface of the anterior left ventricle, where recordings are usually made. This particular multielectrode array, with maximum dimensions of ~6 cm × 11 cm, is sutured at its edges to the anterior left ventricular surface during each experiment.

Higher resolution electrode arrays can be constructed to map fine detail (Fig. 2). The distance between bipoles in this array, shown magnified in the inset, is 1.25 mm. The tips of each bare silver lead (30–32 AWG) are positioned within a plastic mesh attached to a rubberized matrix. Once the leads are in place, they are bonded together with fast-drying glue. The recording surface is then cut and sanded so that the finished electrode contacts (the ends of the bare leads) are planar and the silver metal is exposed. Since this array is not flexible, it is either positioned on the epicardial surface of the heart for short intervals by hand, or the

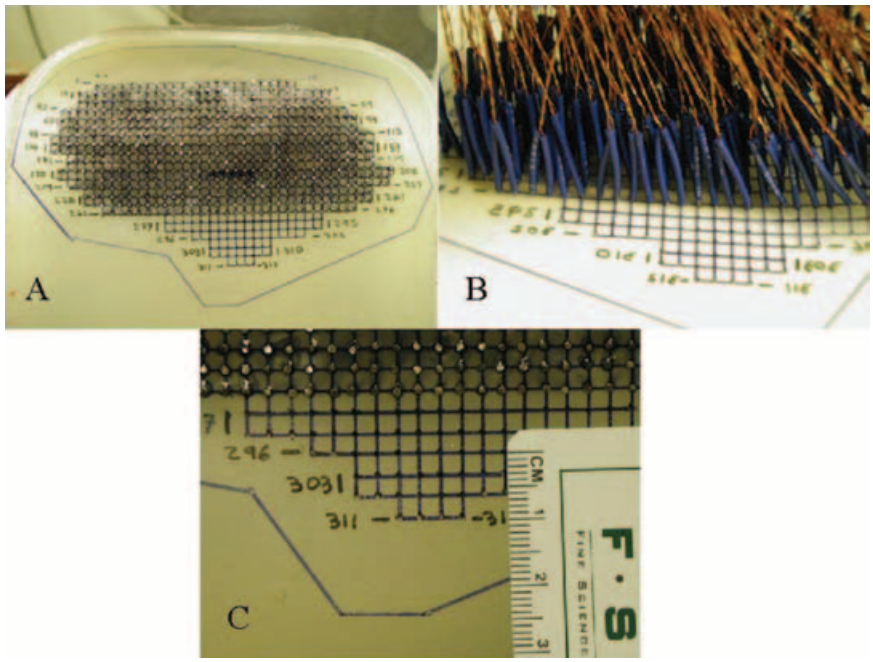

Figure 1. *Construction of a large multielectrode recording array for use in postinfarction canine hearts: (A) electrode side, (B) wire side, and (C) dimension of the square grid.*

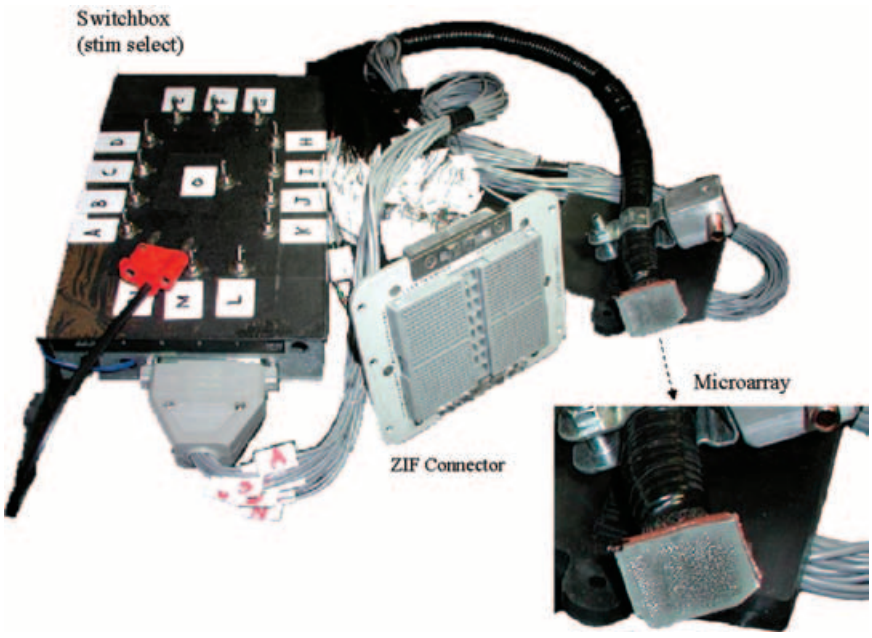

Figure 2. *Microelectrode recording array used for high resolution recordings in postinfarction canine hearts. Inset shows electrode detail.*

position is adjusted with a micromanipulator having multiple degrees of freedom, clamped to the aluminum block adjacent to the array (Fig. 2). A 624-pin zero insertion force (ZIF) connector (Cannon, Inc., USA) is used to provide continuity between the leads of the 312 bipolar multielectrode array and the system electronics. This enables the array to be removed from the system for cleaning following each experiment, and it also provides a rapid disconnect when the heart is to be defibrillated. A switchbox is used to toggle in stimulating electrodes residing along each edge of the array and at its center (Fig. 2). The size of the recording surface is ~2 cm × 2 cm at the longest dimensions.

Following the ZIF connection, the bipolar leads are arranged in sets of 16 for input to 20 data acquisition boards (16 × 20 = 320 channels total). A 37-pin D-shell connector bolted to each data acquisition board is used for the analog signal input. The ECG, blood pressure, and stimulus channel signals are attached directly to the system electronics without a ZIF connecting device.

Preprocessing of the Data

Differential amplifier integrated circuits reside on the data acquisition boards and are used for initial adjustment of the signals and to prevent significant additional noise pickup. Electric and magnetic field capacitative coupling can result in additive noise in the range of micro- to millivolts.[8] By amplifying the millivolt level electrograms by ~100–1,000× in proximity to the recording electrodes, noise pickup prior to amplification is minimized, and noise pickup following amplification is usually not significant because the noise level will then be 100–1,000× less than the electrophysiologic signal. The gain stages are also designed based upon the dynamic range of the analog-to-digital converter (ADC). Surface electrograms typically range from 0.1–10 mV in peak amplitude, and many ADCs typically accept ±10 V inputs. It is important to adjust the final peak-to-peak signal amplitude to the ±10 V input range for maximized digital voltage resolution. When the signal is amplified to this range, all of the discrete voltage levels of the ADC will be utilized in signal conversion. For example, if the ADC has an 8-bit voltage resolution, $2^8 = 256$ discrete voltage levels can be represented. For an allowed input range to the ADC of ±10 V (20 V range), the discrete voltage levels (least significant bit or LSB) are separated by 20/256 = 78 mV; hence each sample point of the analog signal is converted to the nearest 78 mV discrete level. If for example an electrogram with peak-to-peak amplitude of ±5 mV is not amplified at all, at conversion it will be represented by only a single discrete level, and following digital conversion it will appear as a flat signal. If however, this same electrogram is amplified 2,000 times to a final peak-to-peak range of ±10 V, then all 256 discrete voltage levels will be used for its representation during the conversion process. Higher voltage resolution ADCs, for example 16-bit, will provide higher resolution for the same amplified signal

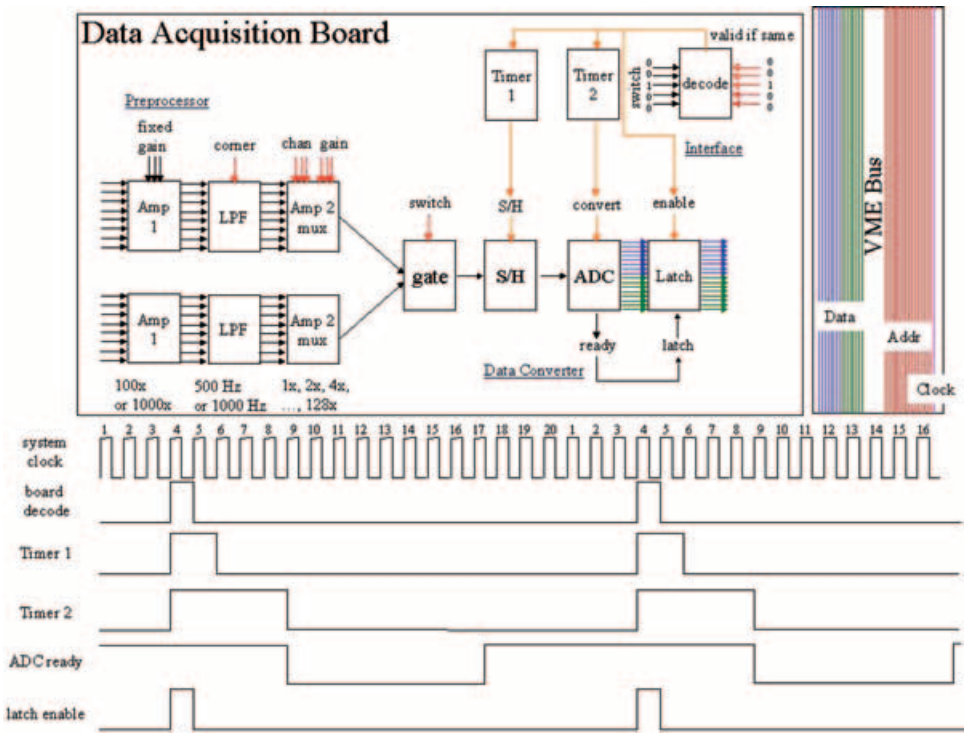

Figure 3. *Block diagram of a multichannel data acquisition board and timing diagram.*

(2^{16} = 65,526 discrete levels; LSB = 20/65,625 = 305 μV).

Analog Amplification

The Amp 1 integrated circuits receive and amplify a total of 16 channels per data acquisition board (Fig. 3, Amp 1). A 100× fixed first stage gain was used to initially amplify the unipolar or bipolar input signals. These are differential amplifiers with two inputs; one input is subtracted from the other so that any component of the signal that is precisely the same on each input will be removed. Motion artifacts or electrical interference having like characteristics at each input, called common mode, are therefore eliminated. If the common mode noise on both inputs is precisely equal, they will be exactly cancelled by the differential amplifier. More commonly, there will be slight differences in amplitude and/or phase in the common mode components at each input. To precisely remove these components requires the use of adaptive noise cancellation.[9–11] When the input signals to the differential amplifier are generated from two closely spaced electrodes on the heart surface (bipolar recording) the output signal comprises mostly deflections due to electrical activity close to the recording sites, because the signal caused by activation of the distant heart mass is mostly common to both inputs and removed during differential amplification. This is desirable for activation mapping in both experimental and clinical settings, so that the local activation time at each recording site can readily be ascertained.[12,13]

A second stage amplifier is also included in the preprocessing circuitry (Fig. 3, Amp 2). Its gain is selected by setting several binary input pins (termed gain-selects) to either a binary high or a low voltage level. Since the pins accept binary inputs, three gain-select pins will provide $2^3 = 8$ possible gain levels. Rather than use the integer numbers 1–8 as gain levels, to increase the range of possible gains, commercially available parts provide for the selection of more widely varying gain levels. For example, if a binary step selection is used, then the eight available gain values would be 1, 2, 4, 8, ..., 128, which would be selected by inputting binary values of 000, 001, 010, ..., 111, respectively, to the gain-select pins. Hence, the signal amplitude, initially at 0.1–10 mV peak-to-peak level, is adjustable to a final level of approximately ±10 V by appropriate stage 1 and 2 amplifications. While stage 1 amplifiers are hardwired to the fixed gain level that is not usually changed, the second stage gain is adjustable during each experiment via an automatic gain control (AGC) algorithm implemented in computer software.

AGC is done by first acquiring short sequences of all signals with Amp 2 gain set to unity (1.0). A commercial data acquisition board (DT2878, Data Translation, Marlboro, MA, USA) acquires the short data sequences from each channel in this system, which are then ported to the DT2878 RAM memory. The appropriate second stage gain is computed from the absolute maximum value m of each signal via an embedded digital signal processor chip. The real number gain g = 10/m, where ±10 is the allowed input range to the ADC in volts. For the binary step second stage amplifier, if g = 24.3 for example, then a second stage gain of 16 (100 binary) would be selected to maximize amplification without exceeding the allowed input voltage range of the ADC.

Analog Filtering

Analog filters are used to remove additive noise and motion artifact and to prevent signal distortion. An active low pass filter (LPF) with 5-pole cutoff eliminates high frequency noise (LPF, Fig. 3). The filter also prevents distortion (aliasing) of the signal by removing signal components $\geq 0.5\times$ the sampling frequency. Any such high frequency components remaining in the signal would not be adequately represented by the discrete sample points (i.e., undersampling would occur) causing a distorted representation of these components (Nyquist theorem).[8] The active LPF is used with a cutoff (corner) frequency of 500 Hz for a minimum sampling rate of 1 kHz. In Figure 3, a binary control line to the LPF, labeled "corner," is used to adjust the cutoff frequency to either 500 or 1,000 Hz via computer software control. Normally it is set to 500 Hz but when sampling at >2 kHz, the 1,000 Hz cutoff can be used.

A high pass filter (HPF) can also be included during preprocessing (not shown). HPFs are used to remove DC bias and motion and breathing artifacts, which are low frequency phenomena.[8] They always remove the mean signal level and set it to 0 V. Therefore, if it is desirable to retain the mean level in the recorded signal, HPF should not be implemented. An example of a simple HPF is an RC circuit with the capacitor (C) positioned in series at the output of Amp 1 in Figure 3 followed by a resistor (R) to ground. Such an RC circuit would make a HPF with a cutoff frequency in Hertz given by $1/2\pi RC$. For $R = 1\ M\Omega$ and $C = 1\ \mu$ farad, the cutoff frequency would be $1/2\pi = 1/6.3s$, or 0.16 Hz, which is suitable to pass significant electrogram components while removing DC bias and reducing motion and breathing artifacts. Real filters do not actually remove all frequencies beyond the cutoff point, but rather, reduce it. This RC circuit is a single pole HPF, meaning that the amplitude at the output is reduced by 20 dB per decade of frequency decrease below the cutoff. Multiple pole filters reduce the output signal level beyond the cutoff frequency by an additional 20 dB per decade of frequency change for each additional pole. Therefore, the 5-pole cutoff LPF (Fig. 3) reduces the output signal level above its cutoff by 100 dB per decade. The simple RC HPF is a "passive" circuit (it is not powered) whereas the LPF circuit of Figure 3 is "active" (powered; power inputs are not shown in the diagram).

Analog Multiplexing

The second stage amplifiers (Amp 2, Fig. 3) also act as 8:1 multiplexers, that is, one of the eight inputs is selected to be present at the output. The three channel select pins (chan, shown for the top Amp 2 only), are used to determine, via software command, which input will be present at the output of this integrated circuit. Following Amp 2 output, the gate shown acts as an additional 2:1 multiplexer, so that the signals are multiplexed 16:1 overall. The switch input to the gate is also driven by a binary (high or low) software command to select one of the two inputs to the output. Multiplexing is done at the preprocessing stage so that only one A/D converter, which is often the single most expensive electronic component in the system, is required on each data acquisition board for digitization of the signals. The analog signals are therefore routed one-by-one to the converter input to be digitized. This sequential digitization of signals is termed "polling," as compared with more expensive systems that use an ADC for each input channel so that simultaneous sampling is achieved.

Analog-to-Digital Conversion

For digitization, the analog signal must be held at a constant level to maintain accuracy during the digitization process. This is done by a sample and hold device (S/H, Fig. 3), which may be integrated as part of the ADC. Initially, the output from the S/H unit follows the input. When a hold command is given to the chip (change from high to low or from low to high binary, depending on the S/H specifications), the output is then held constant at the level of the input at that moment. After a short interval that allows the S/H output to settle, the ADC is commanded to discretize the constant-level analog signal received from the S/H output. Several methods can be used to convert the fixed analog signal level to a digital signal. In the system that was constructed, one bit is converted at a time, from most to least significant, with the time required for conversion of all 16 bits being $\sim 17\ \mu$s.

The 16 binary outputs from the ADC are shown attached to a "Latch" device (Fig. 3; low and high bytes are shown as green and blue lines, respectively). After digitization, the signal is stored

in this temporary memory device for eventual broadcast onto the system data bus. The data are latched, or stored indefinitely, when the converter has finished digitizing an analog signal. The latch output is buffered, i.e., it has the ability to provide (source) a large output current should the load from devices in the peripheral circuitry require it. The load is the current drawn from the set of parallel resistances in the circuitry to which the latch output is connected. As more circuits are connected to the latch output, the resistance is lowered and the load is increased, so that additional current is drawn from the latch. The latch outputs are buffered so that sufficient current is available to supply a large load; otherwise, the voltage level representing a binary "1," or "high," at the outputs would diminish, leading to data errors. The latch is also a tristate device at its output, meaning that in addition to having the capacity for binary output (high or low level), the latch outputs can also be placed in a high impedance state (effectively no connection to peripheral circuitry). This is important because the output leads of the latch are connected to a set of data lines called the system data bus. The latches from all 20 data acquisition boards are connected to the same 16 leads on the data bus to conserve the number of bus lines that must be used for multichannel data acquisition.

To prevent the driving of the system data bus by the latch outputs of more than one data acquisition board simultaneously, termed bus contention, the latch of only one board is placed in the low impedance (binary output) mode at any one time. The broadcast data from each board (digital sample points, each 16-bits wide) are ported sequentially via the system data bus to a data-streaming unit (DT3010, Data Translation) for archival storage to a hard drive or other medium. When a particular data acquisition board is addressed by the system, its "board decode" signal goes high (Fig. 3, bottom), setting off a series of events on the board. Each particular board has its own special number assigned to it; the board shown is "00100" in binary. This number is hardwired or switched into the decode chip (black lines at left on the chip).

The pins on the right side of the decoder are connected to the system address bus. When the number "00100" appears on the address bus, this particular board will be accessed for one system clock cycle (cc). The decode chip output generates a binary "high" pulse at this point (lines in orange connected to Timers and Latch, Fig. 3). The lead connected from the decoder to the latch causes the latch outputs to go to low impedance; therefore the data from this particular board are broadcast onto the system data bus for one system clock cycle (Fig. 3, bottom). Additionally, ADC parameters are set up for the next sample acquisition. Timers are devices that can generate an output pulse of a duration that is selectable by using an external resistor and capacitor (RC circuit). Timer 1 is configured to provide a pulse that is 2 cc in duration when it receives the decoder high signal. The Timer 1 lead is connected to the S/H, and the high pulse commands the S/H to hold the data at its output at a constant level. Timer 2 provides a pulse of longer duration (4 cc), which is connected to the ADC "convert" input pin. The trailing edge of this pulse, 4 cc later, commands the ADC to convert, driving the ADC ready pin low (Fig. 3, bottom). This delay ensures that the output of the S/H chip is stable and ready for digitization. Digitization requires 8.5 cc for the 17 μs conversion time of the ADC, whereupon the ADC ready pin goes high again. Therefore, the system clock as shown is running at 2 μs period = 500 kHz frequency. The ADC ready pin is connected to the Latch command pin, causing the digitized data sample to be latched when the ready pin goes high, so that when the board is next accessed, the new sample point can be broadcast to the system data bus.

The process of accessing a digital sample point sequentially from each board represents a digital multiplex, i.e., a select of data from 1 of 20 data acquisition boards. After all 20 boards have been accessed sequentially, the entire series of steps is repeated so that data from the previous ADC process can be collected. Thus, the overall multiplexing capability of the system selects 1 of 320 channels for broadcast onto the system data bus (1 of 16 analog signals on each data acquisition board followed by selection of a 16-bit digitized signal from one of the 20 boards). The software commands to drive the circuitry of Figure 3 originate from a commercial signal generator board (WSB-10, Quatech Inc., Akron, OH, USA). A set of data points stored in board memory is used to derive the command. The board generates this signal in both analog and digital form, and the digital form is used to drive the system. An example of a binary word (command word) that is generated from the signal generator is:

Board	Channel	Gain	Cutoff
00100	1011	100	0

The first 5 bits from left-to-right designate the data acquisition board that is to be addressed. In this case, the command word is designating board 00100 (board 4 in decimal), depicted in Figure 3. Since there are 20 data acquisition boards in the system, 5 bits, i.e., $2^5 = 32$ different binary numbers, will be sufficient to address the 20 boards.

The five output pins from the signal generator that designate the board number are hardwired to the first five leads of the system address bus, which are in turn connected to the address decoder chip on each data acquisition board via the bus connectors. As described above, when a particular board is accessed, the data stored in the latch are broadcast onto the system data bus. The next 4 bits of the command word above "1011" in binary (11 in decimal) designate the channel number on the board that will be digitized next. These outputs from the signal generator are hardwired to the next four leads on the system address bus, which are in turn connected to the appropriate chips on the board (three to Amp 2 channel input pins and one to the switch input of the gate). The next time the board 4 is addressed, the digitized data from channel 11 will be broadcast onto the system data bus. The gain bits in the command word above, "100" in binary, signify the second stage gain to be used when channel 11 is digitized (amplification of 16× for binary selectable steps from 1–128). These output pins from the signal generator are attached to the next three leads of the system address bus, which are in turn connected to the gain input pins of Amp 2 on each data acquisition board. The last bit "0" in the command word above designates the cutoff frequency of the LPF to be used (500 Hz, whereas a binary "1" would be 1,000 Hz). This is hardwired to the last lead of the system address bus, which is in turn connected to the LPF corner input (Fig. 3, top). Normally during the course of an experiment, the corner frequency bit is held constant for all channels, as is the sampling rate.

The 320 analog channels, 16 on each of 20 data acquisition boards, are accessed by addressing each of them using a distinct command word which is broadcast on the system address bus via the signal generator. A data file containing the set of command words is called up by the signal generator for this purpose. The signal generator is set to run in repeat mode so that the sequence of 320 command words used to access the data are repeated indefinitely until a stop command is given, via a keystroke, at a dedicated PC-type computer within which the signal generator resides. The data file is structured so that the channels are called up by sequentially addressing one per board. First board 1 channel 1, is accessed, then board 2 channel 1, . . . board 20 channel 1, followed by board 1 channel 2, . . . and so on until finally board 20 channel 16. This is done so that the system is configured for maximum data throughput. As described above, the ADC conversion time is ~17 μs, and an approximately 8 μs delay is used for S/H settling (total 25 μs). If all 16 channels on a single data acquisition board were addressed sequentially prior to accessing another board, the minimum time for digitization of all channels would be 25 μs × 16 channels × 20 boards = 8 ms, and the maximum sampling rate per channel would be 1/0.008 s = 125 Hz, which is insufficient to accurately record electrograms and the ECG. However, if one channel per board is accessed sequentially, with acquisition parameters imparted to each, and the resulting digitized sample point obtained on the next access of each board, then the maximum throughput would be ~20× faster, i.e., 2.5 kHz/channel.

Time and Channel Synchronization

In order to ensure that the multichannel digital data can be easily analyzed, a synchronization (sync) module is used to insert time and channel information into the digital data stream. The method for implementation is shown in Figure 4. Synchronization is done by adding a header to the beginning of each 320-channel data block. The data block itself is 640 bytes long for the system as described (320 channels long × 16 bits wide). A 6-byte header is used for synchronization. The first three header bytes are used for time synchronization. These are generated by the 8-bit binary counters shown in Figure 4. Each time the signal generator begins a new repeat of the command word sequence, it provides an output pulse on a dedicated pin. This repeat bit from the signal generator is connected to the input of the "lo" binary counter (Fig. 4) via an additional (14th) lead on the address bus. Each repeat pulse triggers the addition of a binary 1 to the counter, which appears at its output. When the lo counter reaches 11111111, the count turns over on the next repeat pulse to 00000000, and its carry pin emits a pulse which is inputted to the "mid" counter. The process is repeated for the "hi" counter. Thus, 2^{24} repeats of the command sequence can be represented with three 8-bit counters, and the counter outputs are connected to Buffer 1 and half of Buffer 2 (color coded, Fig. 4). The buffer integrated circuits, like latches, can source a large output current and have tristate outputs, however, unlike latches, whatever data are at the inputs always appear at the outputs when in low impedance mode. For a sampling rate of 1 kHz per data block (and therefore 1 kHz per data channel), the total counter capacity represents 4 2/3 hours of time synchronization, which is sufficient for most experiments. These time synchronization bytes designate the time from the beginning of the recording, which is useful during subsequent data analysis. Additionally, channel synchronization words are added to the data stream. A 3-byte flag is used to denote the start of the 320 digitized sample points from one time epoch. The channel synchronization words are shown as 0A, 0B, and 0C (hexadecimal) hardwired to two of

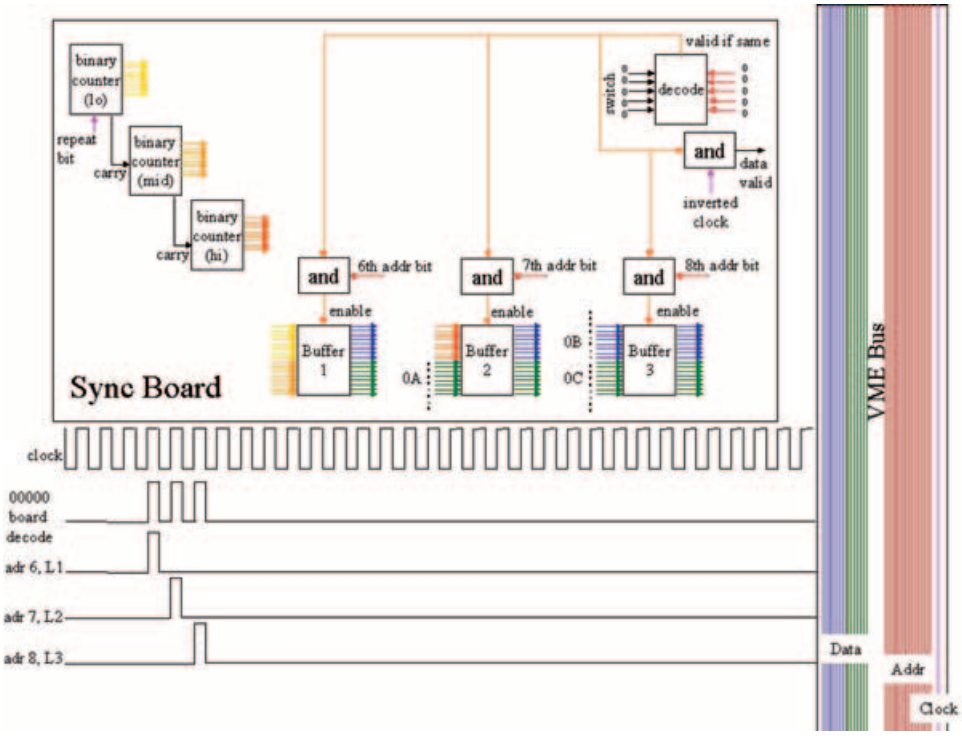

Figure 4. *Block diagram of synchronization board and timing diagram.*

the 16-bit buffers (half of Buffer 2, and Buffer 3, Fig. 4).

The time and channel synchronization bytes are added to the data stream via the tristate buffers (Fig. 4). The color-coded inputs show where the time synchronization bytes are added. When the sync board is accessed (called board 00000), the decode valid signal (high) is sent to one input of the three logical "and" circuits. The other input to each "and" comes from the address bus. Buffer 1 output is enabled (low impedance) when the board is accessed (00000, first five system address bus leads), and the next three leads (6–8) are at binary 001. Buffer 2 is accessed when the board is accessed and leads 6–8 are binary 010, and Buffer 3 when leads 6–8 are 100. Hence, three command words from the signal generator are needed at the start of each data block to insert time and channel synchronization information to the digital data stream:

Board	Latch	x	x
00000	001x	xxx	x
00000	010x	xxx	x
00000	100x	xxx	x

where x denotes that the values of these bits in the command word do not matter (set to 0). Following these three sequential command words, the set of 320 command words which accesses the data acquisition boards are broadcast to the system address bus, beginning with:

Board	Channel	Gain	Cutoff
00001	0000	yyy	0

where the first 5 bits 00001 designate data acquisition board 1, the next 4 bits 0000 designate the first channel on this board is to be accessed, yyy is the gain for this channel, and the last bit 0 indicates that a LPF corner frequency of 500 Hz is being used. Hence, a sequence of 323 command words in total are needed to drive the sync and data acquisition boards, resulting in a multiplexed data stream that is 320 data channels $\times$ 2 bytes wide + 6 bytes header = 646 bytes long per data block.

Real-Time Display

Portions of the digital data stream are displayed in real-time. A display board, which reconverts the digitized signal back to analog form for display, is used for this purpose. Typically, ECG

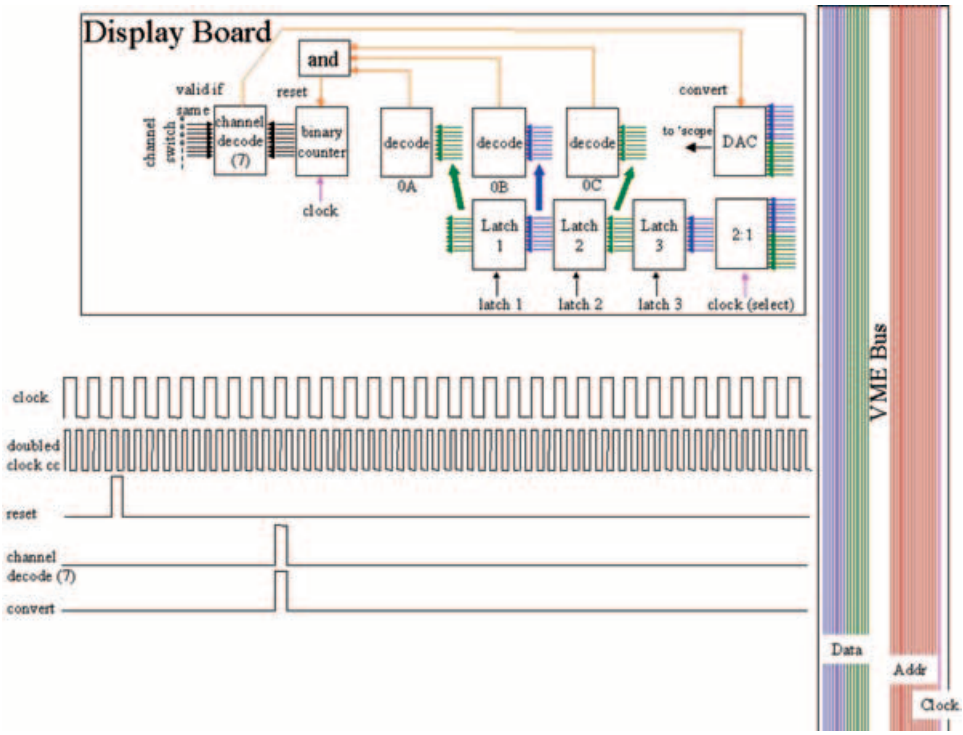

Figure 5. *Block diagram of display board and timing diagram.*

leads I and II, the blood pressure obtained from an indwelling femoral line, the stimulus channel, and a single surface electrogram are displayed for electrophysiologic analysis.[1,4] The data stream is accessed transparently from the system data bus; therefore so long as the signal generator is generating a command sequence, the data will be displayed regardless of whether or not it is simultaneously being streamed to disk.

The process of channel capture for display is illustrated in Figure 5. The 3-byte channel flag word "0A, 0B, 0C" which precedes each set of digitized sample points is first detected. For this purpose, the data stream is inputted to the 2:1 chip (Fig. 5), which selects the high or the low byte to its output (green or blue) based on a high or low level from the system clock. Therefore, a new data byte appears at the 2:1 output at twice the frequency of the system clock (cc). The data are captured by each latch, shown in first in first out fashion. Latches 1–3 are always enabled (low impedance mode). During one double clock frequency cycle, a latch command pulse is inputted to Latch 1, followed by a latch command to Latch 2, and then to Latch 3. The effect is to percolate the data from latch 3 to latch 1. The circuitry to provide the delayed latch commands (not shown) consists simply of three timers, driven by the leading edge of cc, with output pulse widths (binary high) of timer 1 < timer 2 < timer 3 < cc, and the latching occurs on the trailing edge of the timer pulses. When sync words 0A, 0B, and 0C appear on latches 1–3, respectively, each of their three respective decode chips become valid, so that the output of the three-input logical "and" goes high. This high pulse from the "and" resets the binary counter to zero at its output pins. The output pins of the binary counter count up at the rate of the system clock. To display, for example, the seventh digitized data channel (i.e., board 7, first channel), a binary 7 is dialed into the reference inputs of the channel decode chip (left side, Fig. 5). Hence, 7 system clock ticks after the counter is reset (equivalently, 7 clock ticks following the last channel sync word), the channel decode output on the display board will become valid.

This process is illustrated in the timing diagram (Fig. 5, bottom). Seven system clock ticks after the channel flag words appear, the channel decode becomes valid and emits a positive pulse. This valid signal is used to command the digital-to-analog converter (DAC) on the display board to convert the word appearing at the 2:1 inputs at that moment (the 16-bit digital sample from the 7th channel in the data sequence—board 7, channel 1) to analog form for display, which is then sent to an analog oscilloscope or other analog display device. The level of the signal sent to the display only

changes when each new digital data point from the selected channel is converted by the DAC, which is once each millisecond if each data channel is sampled at 1 ms intervals. A single 8-bit channel counter such as is shown for simplicity in Figure 5 can only be used to display one of the maximum of 256 data channels. For the 320 data channel system, a second 8-bit counter (carry bit from first would be connected to count input of second), is used. For display of more than one channel, a separate channel decode and DAC would be needed for each, but only one set of the other components shown on the display board diagram (2:1, channel flag decode, and binary counter) would be needed. Besides display of the signals for analysis, display of the digital data by reconverting to analog form serves as a check that the data is being digitized and synchronized correctly.

System Integration

The components of the system must reside in an environment where they can communicate with each other without signal distortion or noise interference. PC-type computer busses are not designed for fast communication between acquisition boards, and there are a limited number of slots for such boards. The data acquisition cards should be implemented using a fast address bus for broadcast of the command sequence and a fast data bus for broadcast of the header and digital data, which are streamed to disk and displayed. An example of a bus with fast transfer rates is the Versa Module Europa (VME) and its larger capacity version VMEbus eXtensions for instrumentation (VXI),[7] which can provide the necessary data and address lines and power connections, plus the large number of slots necessary for the sync and data acquisition boards (21 slots needed). Although a commercial VME/VXI-based computer with keyboard control can be quite expensive, it is not needed to run this data acquisition system, which is entirely driven by the command sequence from the signal generator.

The VME/VXI bus includes a set of leads for data, addressing, and power, as well as board connectors that are implemented on an electronics board commonly called a backplane or motherboard. For stability and noise reduction, the backplane resides in a metal chassis, or mainframe, and the data acquisition boards, communicating with the bus and therefore with each other via the board connectors, are supported by plastic rails at the top and bottom of the chassis. Besides the mainframe and motherboard, a power supply is needed with sufficient output current to supply all of the boards residing in the chassis. For construction of a 320-channel system (20 boards, 16 channels per board) the power consumed by the data acquisition boards, which have the same components on each board, can be computed by determining the power drawn by a single board and multiplying by 20. The power sinked by a single board is computed by adding the typical power requirement of each active component, which is listed by the manufacturer in the component specifications. Additionally, the drain from the sync board must be computed. The power supply should be chosen so as to provide at least twice the total computed requirement as a margin of error. The chassis should also have a cooling device to prevent overheating of the electronics. One can purchase either a fan plate or individual fans that can be attached to vents at the top or bottom of the chassis. The cooling system need not be loud—noiseless (“whisper”) fans are available at only a small increase in cost. The display board can reside in a separate chassis and requires additional power.

Results

Acquisition of multichannel data for activation mapping is an important tool of the electrocardiologist.[3,14] In Figure 6, examples of epicardial surface electrograms acquired from the infarct border zone in the anterior left ventricle of a postinfarction canine heart are shown using the array detailed in Figure 2. In panel A, the location of each bipolar electrode is given. Signals acquired during normal sinus rhythm in this experiment are displayed in panel B. The channel numbers of the recordings are shown at left (B), and sinus rhythm activation (sharpest deflection) occurs approximately simultaneously at all seven electrode locations shown. The cycle length of the heart was approximately 400 ms during the recording sequence. In panel C, recordings from the same electrodes are shown for the same experiment when the heart was paced at a 260 ms basic cycle length from one edge of the array. Activation at each site is delayed with respect to the stimulus time. At recording sites in proximity to the stimulus site (36 and 40–42, panel A) stimulus artifact can be observed in the recording and activation occurs shortly following the stimulus (C). In panel D, traces were obtained during ventricular tachycardia, and channels 161–165 were located in proximity to the exit of the central common pathway of the reentrant circuit. Channels 319 and 320 are ECG lead traces I and II, respectively. The dashed line (cycle 2) shows the activation sequence for sites 161–165 (D).

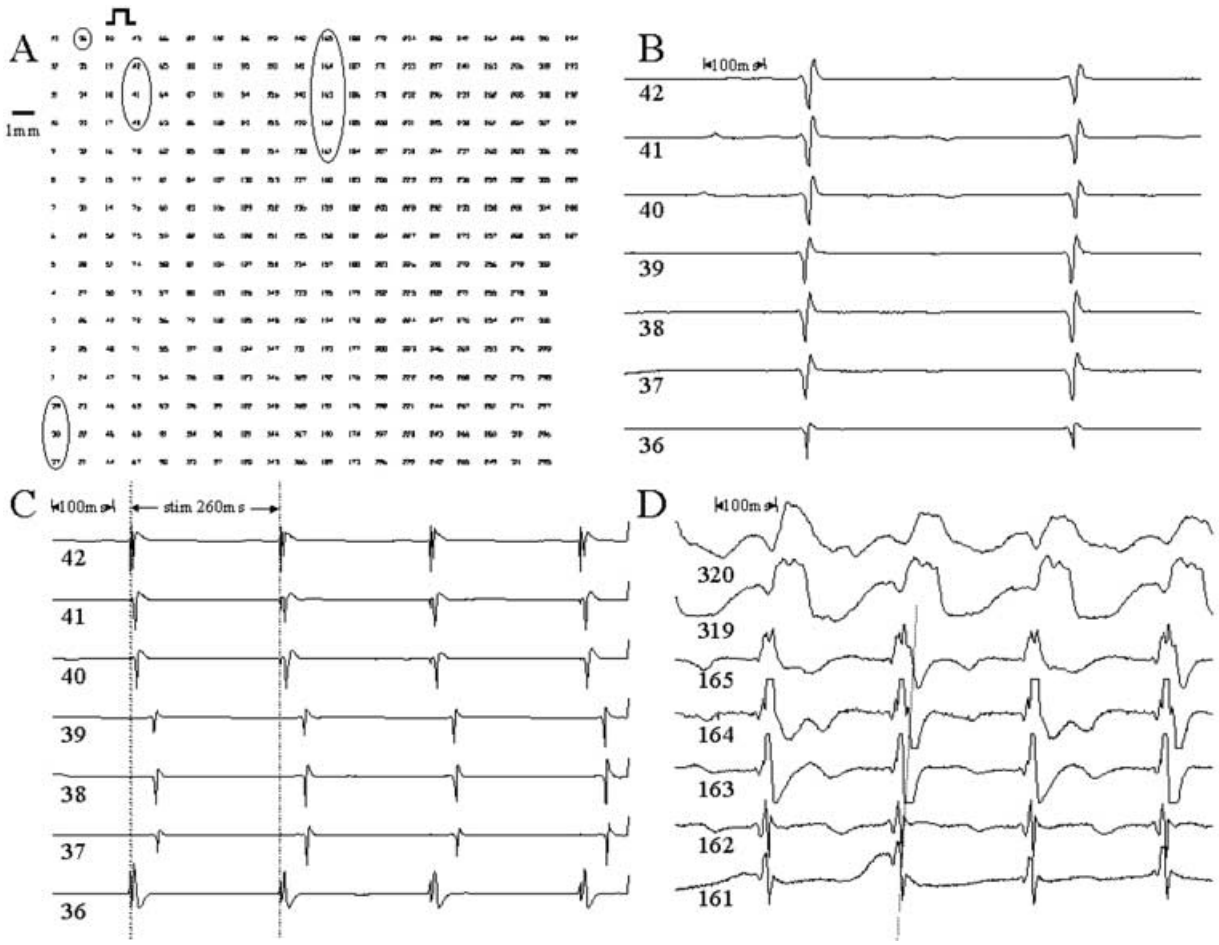

Figure 6. *Example of signals acquired with the array of Figure 2. (A) Grid configuration (B–D) signals acquired with the microelectrode recording array during sinus rhythm, ventricular pacing, and ventricular tachycardia, respectively.*

Discussion

In-House Construction versus Commercial Systems

The system that we have described can easily be implemented using dual in-line package integrated circuits. These components are relatively large thereby providing relative ease in manual soldering, but the cost and board area ("real estate") necessary for implementation are large compared with surface mount components (small outline integrated circuit or SOIC), which are smaller in size and more readily available commercially. A cost analysis was done to determine the total price for implementation of all of the subsystems described in this article. The entire cost of the data acquisition system including integrated circuits and other electronic components, electronic boards and materials needed for their manufacture, VME/VXI bus and chassis, and commercial signal generator and streamer boards housed in dedicated PC computers is approximately $45,000. Implementation with surface mount electronic components would result in substantial cost savings, and additionally, it would be possible to implement a 32 rather than 16-channel count per data acquisition board. By comparison, commercially available turnkey systems having the same capabilities are presently available for approximately $100,000. Such commercial systems are generally proprietary,[7] and onsite support is typically priced at $1,000 or more per visit for time and travel expenses. Hence, if the labor and expertise are available, in-house construction as compared with purchase of a turnkey commercial system is a potentially cost-effective solution for electrophysiologic research applications, with design flexibility, and relative ease of implementation of additional circuitry after construction of the basic system.

Data Resolution

When it is desired to increase the spatial resolution of the multielectrode array, the time

resolution (sampling rate) must also be increased so that higher frequency deflections generated by the closer separation of electrodes can be recorded without distortion.[5] If bipolar electrode recordings are used, the increased time resolution needed to resolve events can be estimated based on the spacing between the poles of the electrode. An activation wavefront traveling 1 mm/ms in a direction parallel to a bipolar electrode pair separated by 1 mm will result in a 1 ms time interval between the peaks of the biphasic deflection, which would require a sampling rate greater than 2/ms (2 kHz) to resolve without distortion.[14] If the spacing between bipolar pairs is 2 mm^2, then a square grid with 100 such bipolar electrodes would be 20 mm $\times$ 20 mm on a side, approximately the same as the average surface area of the central common pathway of reentrant circuits in canine postinfarction studies.[15,16] At a higher spatial resolution of 0.1 mm between electrode bipolar pairs, an activation wavefront traveling 1 mm/ms in a direction parallel to the bipole axis would cross the pair in 0.1 ms. Hence, an approximately 10-fold increase in time resolution would be needed to resolve the resulting biphasic deflection without distortion. If the spatial resolution increases 10$\times$ along the X and Y axes, the total throughput will increase a 1000-fold.

Small-scale deflections in the electrogram become more apparent as voltage resolution is increased. The voltage imparted to a bipolar recording electrode from a distant source is proportional to $1/r^2$, where r is the source-electrode distance.[14,17,18] When the recording electrode bipoles are separated by 1 mm, the mean distance of an activation wavefront traveling between them is 0.5 mm. The maximum dimension of a reentrant circuit is in the order of 30 mm. Hence, based on the $1/r^2$ relationship, near-field versus distant far-field electrogram deflections would have an amplitude ratio of $\sim(0.5/30)^2$, i.e., deflections generated by the distant far-field would be only 0.03% of the amplitude of near-field deflections. For an 8-bit ADC (256 discrete levels) if an AGC is implemented so that the near-field deflections span the allowable input range, distant far-field deflections contained in the same electrogram would span only $256 \times \sim 0.0003 = 0.1$ discrete levels, i.e., less than 1 LSB, and therefore would be unlikely to generate changes in the discretized electrogram shape when the leading edge of the activation wavefront is on the opposite side of the circuit from the recording site. A 16-bit ADC would greatly improve the voltage resolution and could potentially be used to detect distant far-field signals; however, additive noise can be a factor in the least significant bits. Electrogram signals acquired using multielectrode arrays, which are related spatially according to electrode location, can be quantified using image as well as signal processing techniques.[19]

Limitations

Commercial integrated circuits and their specifications change over the course of a few years, so that parts currently being manufactured have the potential to rapidly become obsolete. Legacy components, i.e., those that are no longer being commercially manufactured on a regular schedule, can often be purchased as leftovers or used materials, or even manufactured in large quantities, via specialized companies, but at high cost. Although the multichannel data acquisition system as described is useful for animal research, it does not contain the safety components (electrical isolation) that would be necessary for human use.[8] The impact of many metal electrode disks on the normal conduction of the heart is not entirely known. Use of optical recording techniques can be used to acquire data without metal-tissue interaction.[20]

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References

1. Dillon SM, Allessie MA, Ursell PC, Wit AL. Influences of anisotropic tissue structure on reentrant circuits in epicardial border zone of subacute canine infarcts. Circ Res 1988; 63:182–206.
2. Ciaccio EJ. Analysis and acquisition of multichannel data in electrocardiology. IEEE Eng Med Biol Mag 1998; 17:32–33.
3. Ershler PR, Steadman BW, Moore KB, Lux RL. Systems for measuring and tracking electrophysiologic distributions. IEEE Eng Med Biol Mag 1998; 17:56–61.
4. Wit AL, Janse MJ. Basic mechanisms of arrhythmias. In: Wit AL, Janse MJ (eds.): The Ventricular Arrhythmias of Ischemia and Infarction. New York, NY, Futura, 1993, pp. 1–160.
5. Rogers JM, Bayly PV, Ideker RE, Smith WM. Quantitative techniques for analyzing high-resolution cardiac-mapping data. IEEE Eng Med Biol Mag 1998; 17:62–72.
6. Bove RT, Dillon SM. Optically imaging cardiac activation with a laser system. IEEE Eng Med Biol Mag 1998; 17:84–94.
7. Malkin RA. Constructing a multichannel electrocardiography system from a few standardized, high-level components. IEEE Eng Med Biol Mag 1998; 17:34–38.
8. Webster JG (ed.). Medical Instrumentation: Application and Design. New York, Wiley, 1997, pp. 1–60.
9. Ciaccio EJ, Wit AL, Scheinman MM, Dunn SM, Akay M, Coromilas J. Prediction of the location and time of spontaneous termination of reentrant ventricular tachycardia for radiofrequency catheter ablation therapy. J Electrocardiol 1995; 28(Suppl.):165–173.
10. Ciaccio EJ, Scheinman MM, Fridman V, Schmitt H, Coromilas J, Wit AL. Dynamic changes in electrogram morphology at functional lines of block in reentrant circuits during ventricular tachycardia

in the infarcted canine heart. J Cardiovasc Electrophysiol 1999; 10:194–213.
11. Ciaccio EJ. Localization of the slow conduction zone during reentrant ventricular tachycardia. Circulation 2000; 102:464–469.
12. Ino T, Fishbein MC, Mandel WJ, Chen PS, Karagueuzian HS. Cellular mechanisms of ventricular bipolar electrograms showing double and fractionated potentials. J Am Coll Cardiol 1995; 26: 1080–1089.
13. de Groot NMS, Schalij MJ, Zeppenfeld K, Blom NA, Van der Velde ET, Van der Wall EE. Voltage and activation mapping: How the recording technique affects the outcome of catheter ablation procedures in patients with congenital heart disease. Circulation 2003; 108:2099–2106.
14. MacLeod RT, Brooks DH. Recent progress in inverse problems in electrocardiology. IEEE Eng Med Biol Mag 1998; 17:73–83.
15. Ciaccio EJ, Costeas C, Coromilas J, Wit AL. Static relationship of cycle length to reentrant circuit geometry and to the SCZ during ventricular tachycardia. Circulation 2001; 104:1946–1951.
16. Ciaccio EJ, Tosti AC, Scheinman MM. Relationship between sinus rhythm activation and the reentrant ventricular tachycardia isthmus. Circulation 2001; 104:613–619.
17. Spach MS, Miller WT III, Miller-Jones E, Warren RB, Barr RC. Extracellular potentials related to intracellular action potentials during impulse conduction in anisotropic canine cardiac muscle. Circ Res 1979; 45:188–204.
18. Plonsey R, Barr RC. Bioelectricity. A Quantitative Approach, 2nd Ed. New York, Kluwer Academic, 2000, pp. 217–243.
19. Russ JC. The Image Processing Handbook. Boca Raton, CRC Press, 1995, pp. 151–406.
20. Dillon SM, Kerner TE, Hoffman J, Menz V, Li KS, Michele JJ. A system for in-vivo cardiac optical mapping. IEEE Eng Med Biol Mag 1998; 17:95–108.